PRASADRAM S

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SUMMARY

- About 19+ years of experience in safety critical embedded SW development for global product R&D.
- Strong hands-on Technical Leader | Certified in Cybersecurity & Functional Safety | SAFe Agilist

EXPERIENCE

SW ARCHITECT, L & T Technology Services (Sep 2024 to Dec 2024)

- Created outline concept for brain ECU with Classic/Adaptive AutoSAR ECUs connected via Ethernet/SOME IP.
- Interfaced with global teams for Program Increment (PI) planning on the Agile Release Train (ART), managed local sprints along with IBM EWM workflow integration.

Sr. TECH ARCHITECT, HCLTech (Jan 2019 to Sep 2024)

- Defined the SW architecture for implementing UDS protocol (ISO 14229) on a Renesas RH850 based legacy ECU.
- Provided hands on technical leadership to a team of 4, delivered 30% ahead of time and reduced development costs by 60%.
- Ported freeRTOS kernel on RH850 based ECU, improved platform SW by a façade design pattern-based HW abstraction.

Sr. TECH ARCHITECT, HCLTech JAPAN (Aug 2019 to Apr 2021)

- Created outline SW designs for Software components (SW-C) Test SWC, COM Error Handler SWC on AutoSAR based ECU. This led to increased customer confidence on developing/deploying new SW- Components at Application layer.
- Designed threadsafe, re-entrant middleware SW libraries on Freescale iMX257 target ECU / uITRON4 kernel for Tractor HMIs.
- Created SW Safety analyses using IEC 61784-3 fieldbuses for CAN black channel in stairlift firmware (SIL 2).
- Awarded Individual Best Performer by customer for architecture / code deliveries for year 2020.

SW ARCHITECT, ALSTOM TRANSPORT (Jun 2017 to Dec 2018)

- Built and managed a team of 4 members for the SIL4 SW Integration tests in Test campaign on Alpha releases.
- Created Application protocols architecture concept and safety layer black channel (EN 50159).
- Provided technical leadership to a team of 4 developers in developing a M out of N(MooN) Simulator based PC Application.
- Product & Platform - Safety Computer having 2 x (2 Out Of 2) Composite fail safe dual channel architecture running on Multicore CPU / PikeOS Hypervisor, Time / Space partitioning with CENELEC EN 50128 / RAMS.

MANAGER I, SIEMENS (Sep 2011 to Jun 2017) – Worked in various roles/ international locations.

FIRMWARE ARCHITECT (Apr 2015 to Jun 2017)

- Defined a preliminary SW architecture for integration of LoRa radio module / LoRaWAN stack to Fault passage indicator (FPI).
- Technically led a team in prototyping LoRa prototyping using Semtech SX1278 COTS module.
- Ported Micrium µCOSIII kernel on a Freescale Kinetis K10 for new bring up.

PRINCIPAL ENGINEER- SW, SIEMENS UNITED KINGDOM (Mar 2013 to Apr 2015)

- Defined HAL layer for Tricore / Cortex M4 platform, integrated freeRTOS and developed OS Abstraction layers.
- Analysed and fixed PR / CRs on Platform and Communication SW components in legacy Control & Protection devices.
- Long-term deputation to UK R&D Centre aimed at technical transfer of SIEMENS Control & Protection products.

FIRMWARE MANAGER, SIEMENS (Oct 2011 to Mar 2013)

- Ported Micrium µCOSII kernel on Blackfin DSP, developed platform SW drivers and integrated COM stacks- IEC101/104.
- Led a team (6-8) for developing parameterization, bootloader, fail safe voter and HTTP server for SICAM CMIC Redundancy solution (SIL2-IEC 61508).
- As Sub PM - firmware, successfully performed insourcing of RTU deliverables from contractors for NPI / NPD in Agile-LEAN.
- Built the firmware team, infrastructure/tools from scratch and ramped up the team size to 20.
- Identified 3rd party COTS libraries for make-buy decisions for improved platform sustenance in Common platform projects.
- Worked for a long term in Siemens Austria centre for Project establishment, topics on SW Requirements and Architecture.

Sr. Engineer (R&D), CE+T POWER (Mar 2010 to Sep 2011)

- Implemented CANopen protocol and CANopen bootloader via Service data objects (SDO) upload/download mechanism by integrating stack from PORT GmbH.
- Developed modBUS and CAN management libraries, integrated firmware into the Inverter target (ST ARM9 micro).
- Worked in Belgium for a long term for SW development / Integration work packages.

SR. SW ENGINEER, ABB CORPORATE RESEARCH (Jul 2005 to Oct 2008)

- Developed Distributed Network Protocol (DNP3) stack using C++/Vxworks 5.5.
- Designed middleware libraries for Trend/Alarm subsystem, unit tested achieving 90% coverage.
- Designed Vxworks drivers for SPI flash and RS485 on a PowerPC custom board.
- Worked for a long term in Sweden for development / SW integration.

ENGINEER - Design & Development, TATA Elxsi (Dec 2004 to Jun 2005)

- Developed RTP/RTSP multithreaded applications on ARM9 / Linux for Consumer multimedia projects.

SW ENGINEER, L&T EmSyS (Jul 2004 to Oct 2004)

- Enhanced platform SW on Vxworks 5.4/ PowerPC custom target on a Patient Monitor device.

RESEARCH ENGINEER/FELLOW, DRDO (Feb 2003 to Jul 2004)

- Developed low level drivers in Vxworks 5.4 / PowerPC in a controlled DoD-STD-2167A process.

SKILLS

- Programming: Embedded C/ RTOS, Platforms: 32-bit Microcontrollers, multi-core CPU
- Protocols: CAN, SPI, RS485, Industrial Communication: DNP3, Modbus, CANopen, IEC 101/104
- Automotive specific: BSW MCAL, UDS, CAN-FD, GENy, Debuggers: Lauterbach TRACE32, JTAG
- End Products: Engine control / Zonal / AutoSAR/ legacy ECU, Rail Signalling- CBTC
- Industrial Automation- Control & Protection Relays, RTUs, IO controllers, Power Control products, MedTech devices

EDUCATION

- PG Certificate Embedded Systems Design, University of Pune, India, B+ Grade
- Bachelor of Engineering (Electronics & Instrumentation), R V College of Engineering, Bangalore, First Class

CONTINUOUS LEARNING & PROFESSIONAL CERTIFICATIONS

- INCOSE – ASEP System Engineering certification (in progress) – since Jul 2025
- Automotive Cybersecurity Professional (CACSP) - ISO 21434 till (up to Jul.29) – Znumber 1294

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- Automotive Functional Safety (AFSP) - ISO 26262 (up to May 29) – Znumber 4714

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- Certified SAFe Agilist, Scaled Agile Inc., since Aug 2018
- CEP Certificate course in Project Management, IIT Delhi / PMCC - 2018
- GitHub link- https://github.com/prasa9

AWARDS

Government of India Scholar- Belgium Government Fellowship for higher studies in Electronics Engineering - 2009