Shrisha PRASAD RAM

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ABOUT ME

- 19+ years of Experience in safety critical Embedded Software / Firmware as an Architect and Individual Contributor - developer & Strong hands on Technical Leader | Certified in Automotive Cybersecurity & Functional Safety from TUV Saar | SAFe Agilist
- Eligible for EU Blue Card and Visa Sponsorship. Relocation to Germany supported by The Expat Concept. Available immediately.
- Extensive international experience working in EU for global projects.

WORK EXPERIENCE

SW ARCHITECT, L & T TECHNOLOGY SERVICES – 09/2024 – 12/2024

- Technically led a 12-member team to define SYS level requirements for the Vehicle/Safety functions and create static and dynamic architecture in Rhapsody / map and update Interface signals (ETH / SOME- IP). The zonal E/E architecture has combined AUTOSAR Adaptive and Classic ECUs connected via Ethernet.
- The platform ECU is based on multi-core CPU running QNX Hypervisor. Interfaced with cross functional global teams for PI planning on the ART, collaborated for IBM EWM ALM workflow integration along with leading the local sprints. Acquired IBM Rhapsody specialist certification for SysML v8.

HCLTECH

SR. SW ARCHITECT - EMBEDDED – 14/01/2019 – 01/09/2024

- Specified the SW architecture, provided hands on technical leadership to a team of 3-4 members in implementing UDS protocol (ISO 14229) on a legacy ECU based on Renesas RH850. Refined the existing CAN driver, reused CAN-Tp layer from legacy platform, delivered 30% ahead of time and reduced development costs by 60%.
- Created preliminary outline SW designs for Software components (SW-C) Test SWC, COM Error Handler SWC for handling the CAN timeout errors. This quick proof of concept led to increased customer confidence on creating new SW-Component at Application layer.

HCLTech JAPAN (2019-2021)

- Stationed at OEM location in Japan as SW - Architect / onsite coordinator on development/Acceptance test topics in a Vcycle. Awarded Individual Best Performer by customer for architecture/ code deliveries for year 2020.
- Enhanced the legacy platform SW architecture by façade design pattern-based HAL for Platform SW, ported freeRTOS on RH850 based ECU, improved platform SW by adding abstraction layer over the real time kernel.
- Designed threadsafe and re-entrant middleware SW libraries on Freescale iMX257 target ECU / uITRON4 kernel for Tractor HMIs.Created SW Safety analyses as per IEC 61784-3 Functional safety fieldbuses for CAN communications black channel in Stairlift elevator product firmware (SIL 2).

SW ARCHITECT - EMBEDDED, ALSTOM TRANSPORT – 06/2017 – 04/2018

- Built and managed a team of 4 members for the SIL4 SW Integration tests for Test campaign on Alpha releases.
- Created Application protocols architecture concept and safety layer black channel (EN 50159). Platform is Safety computer having 2 x (2 Out Of 2) Composite fail safe dual channel architecture running on Multicore CPU / PikeOS Hypervisor with Time / Space partitioning. Product: Alstom CBTC solution U400 with CENELEC EN 50128 / RAMS.
- Provided technical leadership to a team of 3 developers in developing a M out of N(MooN) Simulator as LXC container- based PC App that emulated the actual SIL4 Safety computer.

FIRMWARE ARCHITECT / MANAGER, SIEMENS – 10/2011 – 06/2017

- FIRMWARE ARCHITECT (Apr 2015 to Jun 2017) - Defined a preliminary SW architecture for integration of LoRa radio module / LoRaWAN protocol stack to the Fault passage indicator (FPI) - used to detect phase faults and earth faults in medium-voltage cable networks. Technically led a team in prototyping using Semtech SX1278 COTS.
- Ported Micrium µCOSIII III kernel on a Freescale Kinetis K10 target for new bring up. As Re-use correspondent for global Embedded SW Re-use project, closely collaborated with PO/Architects in Germany for SW Architecture, COTS/legacy SW re use libraries deployment in Design to Cost (DTC) projects.

Principal Engineer - SW, Siemens UK R&D Centre (2013-2015)

- Created hardware abstraction layer for Tricore / Cortex M4 custom HW, introduced RTOS support in platform software by defining OS Abstraction layer, ported and integrated freeRTOS, analysed and fixed PR / CRs on Platform and Communication SW components in legacy Control & Protection devices (Reyrolle/Siprotec branded Intelligent Electronic Devices).
- Long-term deputation to UK R&D Centre aimed at technical transfer of SIEMENS Control & Protection products with UK and German teams.

Firmware Manager, Siemens (2011-2013)

- Technically lead a team of 8 developers for developing fail safe voter redundancy, embedded webserver apps and integrating Comm.stack (SMSC lan92xx ETH chip /Fusion TCP/IP stack/HTTP stack, IEC 60870-5-104,101 libraries) middleware/application, customised rules in PC Lint for Blackfin DSP builds.
- The SW/HW development relies on the SICAM CMIC module (RTUs used for Secondary Distribution Automation) based Redundancy solution used for Turbine control applications that are redundant, with high-availability and fault-tolerant / safety integrity levels up to SIL2 (IEC 61508). As SubPM -Firmware, successfully performed insourcing of Feeder RTU from 3rd party contractors, sustenance and enhancement activities and NPI/NPD.
- Worked on a long term in Siemens Austria on SW architecture definition and development tasks in accordance to SIL2 (IEC 61508), ported Micrium µCOSII Real time kernel on Blackfin DSP, developed platform SW and COM stacks. Built from scratch the firmware team and ramped up team size to 20, identified 3rd party COTS libraries for make/buy decisions that led to improved platform sustenance. The projects used an Agile-LEAN techniques for NPI/NPD/Sustenance.

SR.SW ENGINEER, CE+T BELGIUM – 03/2010 – 09/2011

- Implemented CANopen protocol using stack from PORT Gmbh, optimised CPU cycles by 3x and achieved small code size by 2x, developed CANopen bootloader via Service data objects (SDO) upload/download mechanism.
- Developed modBUS and CAN management modules and integrated into the Inverter codebase.
- Worked in Belgium on a long term for SW development/Integration work packages. End product is a Modular inverter with N+1 redundancy for telecom applications.

SR.SW ENGINEER, ABB CORPORATE RESEARCH – 07/2005 – 10/2008

- Designed Vxworks drivers for SPI flash and RS485, optimized driver functionality by adding handling echo, collision avoidance/ detection and resend for interrupt driven scenario with 2-wire mode.
- Developed Distributed Network Protocol (DNP3) stack using C++/Vxworks 5.5 on a PowerPC target, implemented observer design pattern for the protocol event subsystem, designed middleware libraries for Trend/Alarm handling subsystem, unit tested achieving 90% coverage.
- Worked for a long term in Sweden for development/SW integration. Products: Power System protection Substation Automation
- Products ABB REx670, TEC, 800xA ABB Distributed Control Systems

ENGINEER- DESIGNR, TATA ELXSI – 12/2004 – 06/2005

- Developed threadsafe re-entrant libraries for RTP/RTSP multithreaded applications on ARM9 / Linux.

SW ENGINEER, LARSEN & TOUBRO EMSYS – 07/2004 – 10/2004

- Enhanced platform SW on Vxworks 5.4/ PowerPC custom target / Diab C for Firmware sustenance tasks on medical devices.

RESEARCH ENGINEER FELLOW, DRDO GOVERNMENT OF INDIA – 02/2003 – 07/2004

- Developed and technically documented platform SW low level drivers in VxWorks 5.4 / PowerPC for Aerospace systems in a controlled DoD-STD-2167A process for LCA (Light Combat Aircraft) program.

EDUCATION AND TRAINING

PG CERTIFICATE IN EMBEDDED SYSTEMS DESIGN, UNIVERSITY OF PUNE, B+ GRADE

BACHELOR OF ENGINEERING IN ELECTRONICS & INSTRUMENTATION, RV COLLEGE OF ENGINEERING, FIRST CLASS

AUTOMOTIVE FUNCTIONAL SAFETY (AFSP) - ZNUMBER 4714, HTTPS://SGS-TUEV-SAAR.COM/EN/TRAININGS-CERTIFICATIONS/CERTIFICATIONS/CERTIFICATE-DATABASE/PERSONS/TYPE/AFSE

AUTOMOTIVE CYBERSECURITY PROFESSIONAL (CACSP) – ZNUMBER 1294, HTTPS://SGS-TUEV-SAAR.COM/EN/TRAININGS-CERTIFICATIONS/CERTIFICATIONS/CERTIFICATE-DATABASE/PERSONS/TYPE/CACSP

PROJECT MANAGEMENT AS PER PMBOK5 FROM IIT DELHI/ PMCC

INCOSE ASEP - SYSTEMS ENGINEERING PROFESSIONAL (CURRENT)

SAFE AGILIST, SCALED AGILE INC.

SKILLS

Microsoft Office package: Microsoft Word, Excel, PowerPoint, Access | C, RTOS, Embedded SW, Firmware, Microcontrollers, SW Architecture Patterns, Team leading | firmware | use software design patterns | design firmware | define software architecture | lead a team | Agile project management | ICT communications protocols | embedded systems | software frameworks | develop ICT device driver | analyse software specifications | debug software

HONOURS AND AWARDS

Erasmus Mundus Master of Science in Photonics

Belgium Government fellowship for Masters of Science in Photonics engineering in 2009