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ABOUT ME

- 19+ years of Experience in safety critical Embedded Software / Firmware as an Architect and Individual Contributor - developer & Strong hands on Technical Leader | Certified in Automotive Cybersecurity & Functional Safety from TUV Saar | SAFe Agilist
- Extensive internaitonal work experience in the European region for global projects in cross cultural environment.

WORK EXPERIENCE

L & T TECHNOLOGY SERVICES – BANGALORE, INDIA

SOFTWARE ARCHITECT - EMBEDDED – 01/09/2024 – 12/11/2024

- Managed 12-member team in defining SYS level requirements in DOORS DNG for the Vehicle/Safety functions, static and dynamic architecture definition in Rhapsody / mapping/ updating Interface signals (ETH / SOME- IP). Interfaced with cross functional global teams for PI planning on the ART, collaborated for IBM EWM ALM workflow integration along with leading the local sprints. The Zonal E/E architecture has combined AUTOSAR Adaptive and Classic ECUs connected via Ethernet.
- The platform ECU is based on multi-core CPU running QNX Hypervisor. Acquired IBM Rhapsody specialist certification for SysML V8.

HCLTECH – BANGALORE, INDIA

SR. SW ARCHITECT - EMBEDDED – 14/01/2019 – 01/09/2024

- Specified the SW architecture, provided hands on technical leadership to a team of 3-4 members in implementing UDS protocol (ISO 14229) on a legacy ECU based on Renesas RH850. Refined the existing CAN driver, reused CAN-Tp layer from legacy platform, delivered 30% ahead of time and reduced development costs by 60%. Created preliminary outline SW designs for Software components (SW-C) Test SWC, COM Error Handler SWC for handling
- the CAN timeout errors. This quick PoC led to increased customer confidence on creating new SW-Cs at Application layer.
- Legacy ECU topics: Technically lead a team to a team in migrating legacy PF based on Renesas R8C to NXP S32 platform SW components.
- provided technical leadership to develop UDS Server protocol stack per ISO 14229, with adaptation to CAN low level driver and CanTp (15765-2) layers from existing PF, refining platform driver interfaces to be AutoSAR styled interfaces, unit testing in VectorCAST after modification.
- Created façade pattern-based HAL for Platform SW, ported freeRTOS kernel on RH850 based ECU, implemented freeRTOS abstraction layer, implemented abstraction API with sample application.
- Ensured there is no degradation in static analysis results, code coverage,100% requirements traceability for all modules in all the sub-systems modified/developed on legacy platform.
- implemented middleware SW libraries on Freescale iMX257 target ECU / µITRON4 kernel for Tractor HMIs.
- Created SW Safety analyses as per IEC 61784-3 Functional safety fieldbuses for CAN communications in Stairlift elevator product firmware (SIL 2).

HCL Japan - 2019-2021

- Stationed at OEM location in Japan as SW - Architect / onsite coordinator on development/Acceptance test topics in a Vcycle.
- Awarded Individual Best Performer by customer for architecture/ code deliveries for year 2020.
- Enhanced the legacy platform SW architecture by façade design pattern-based HAL for Platform SW, ported freeRTOS onRH850 based ECU, improved platform SW by adding abstraction layer over the real time kernel.
- Designed threadsafe and re-entrant middleware SW libraries on Freescale iMX257 target ECU / µITRON4 kernel for Tractor HMIs.Created SW Safety analyses as per IEC 61784-3 Functional safety fieldbuses for CAN communications black channel in Stairlift elevator product firmware (SIL 2).

ALSTOM TRANSPORT – BANGALORE, INDIA

SOFTWARE ARCHITECT - EMBEDDED – 27/06/2017 – 26/04/2018

- Built and managed a team of 4 members for the SIL4 SW Integration tests for Test campaign on Alpha releases.
- Created Application protocols architecture concept and safety layer black channel (EN 50159). Platform is Safety computer having 2 x (2 Out Of 2) Composite fail safe dual channel architecture running on Multicore CPU / PikeOS Hypervisor with Time/ Space partitioning. Product: Alstom CBTC solution U400 with CENELEC EN 50128 / RAMS
- Provided technical leadership to a team of 3 developers in developing a M out of N(MooN) Simulator as LXC container- based PC App that emulated the actual SIL4 Safety computer. Tools /Techniques: CODEO IDE, TRACE32, DOORS, ClearCase, QA-C, MISRA C 2012, CENELEC EN 50128 / 50159 / RAMS

SIEMENS – BANGALORE, INDIA

FIRMWARE ARCHITECT MANAGER – 03/10/2011 – 14/06/2017

- FIRMWARE ARCHITECT (Apr 2015 to Jun 2017)
- Defined a preliminary SW architecture for integration of LoRa radio module /LoRaWAN protocol stack to the Fault passage indicator (FPI) - used to detect phase faults and earth faults in medium-voltage cable networks.Technically led a team in prototyping using Semtech SX1278 COTS.
- Ported Micrium µCOSIII III kernel on a Freescale Kinetis K10 target for new bring up. As Re-use correspondent for global Embedded SW Re-use project, closely collaborated with Product Owner /System Architects in Germany for SW Architecture definition, COTS/legacy SW re use libraries deployment in Design to Cost (DTC) projects.

Principal Engineer - SW, Siemens UK R&D Centre (2013-2015)

- Created hardware abstraction layer for Tricore / Cortex M4 custom HW, introduced RTOS support in platform software by defining OS Abstraction layer, ported and integrated freeRTOS, analysed and fixed PR / CRs on Platform and Communication SW components in legacy Control & Protection devices (Reyrolle/Siprotec branded Intelligent Electronic Devices).
- Long-term deputation to UK R&D Centre aimed at technical transfer of SIEMENS Control & Protection products with UK and German teams.

Firmware Manager, Siemens (2011-2013)

- Technically lead a team of 8 developers for developing fail safe voter redundancy, embedded webserver apps and integrating Comm.stack (SMSC lan92xx ETH chip /Fusion TCP/IP stack/HTTP stack, IEC 60870-5-104,101 libraries) middleware/application, customised rules in PC Lint for Blackfin DSP builds.
- The SW/HW development relies on the SICAM CMIC module (RTUs used for Secondary Distribution Automation) based Redundancy solution used for Turbine control applications that are redundant, with high-availability and fault-tolerant / safety integrity levels up to SIL2 (IEC 61508). As SubPM -Firmware, successfully performed insourcing of Feeder RTU from 3rd party contractors, sustenance and enhancement activities and NPI/NPD.
- Worked on a long term in Siemens Austria on SW architecture definition and development tasks in accordance to SIL2 (IEC 61508), ported Micrium µCOSII Real time kernel on Blackfin DSP, developed platform SW and COM stacks. Built from scratch , the firmware team and ramped up team size to 20, identified 3rd party COTS libraries for make/buy decisions that led to improved platform sustenance. The projects used an Agile-LEAN techniques for NPI/NPD/Sustenance.

CE+T BELGIUM – CHENNAI, INDIA

LEAD SOFTWARE ENGINEER – 01/03/2010 – 01/09/2011

- Implemented CANopen protocol using stack from PORT Gmbh, optimised CPU cycles by 3x and achieved small code size by 2x, developed CANopen bootloader via Service data objects (SDO) upload/download mechanism. Developed modBUS and CAN management modules and integrated into the Inverter codebase.
- Worked in Belgium on a long term for SW development/Integration work packages. End product is a Modular inverter with N+1 redundancy for telecom applications.

ABB CORPORATE RESEARCH – BANGALORE, INDIA

SR.SOFTWARE ENGINEER – 01/07/2005 – 18/10/2008

- Designed Vxworks drivers for SPI flash and RS485, optimized driver functionality by adding handling echo, collision avoidance/ detection and resend for interrupt driven scenario with 2-wire mode.
- Developed Distributed Network Protocol (DNP3) stack using C++/Vxworks 5.5 on a PowerPC target, implemented observer design pattern for the protocol event subsystem, designed middleware libraries for Trend/Alarm handling subsystem, unit tested achieving 90% coverage.
- Worked for a long term in Sweden for development/SW integration. Products: Power System protection Substation Automation. Products ABB REx670, TEC, 800xA ABB Distributed Control Systems

TATA ELXIS – BANGALORE, INDIA

SOFTWARE DESIGN ENGINEER – 12/12/2004 – 01/06/2005

- Individual contributor - Multithreaded development on a 32-bit ARM platform.
- Techniques: RTP / RTSP, AMR Audio, MP TS / MP4 V

LARSEN AND TOUBRO EMSYS – MYSORE, INDIA

SOFTWARE ENGINEER – 21/07/2004 – 07/10/2004

- Individual contributor role for driver development under Vxworks 5.4/ PowerPC custom target (IEC62304-Class B device), Diab C

DRDO GOVERNMENT OF INDIA – BANGALORE, INDIA

RESEARCH FELLOW – 20/02/2003 – 14/07/2004

- Developed and technically documented platform SW low level drivers in VxWorks 5.4 / PowerPC for Aerospace systems in a controlled DoD-STD-2167A process for LCA (Light Combat Aircraft) program.

EDUCATION AND TRAINING

01/01/2002 – 01/01/2003 PUNE, India

PG CERTIFICATE IN EMBEDDED SYSTEMS University of Pune

Website http://www.unipune.ac.in/

01/11/1997 – 01/11/2001 Bangalore, India

BACHELOR OF ENGINEERING IN ELECTRONICS INSTRUMENTATION RV College of Engineering

Website https://www.rvce.edu.in/

AUTOMOTIVE FUNCTIONAL SAFETY PROFESSIONAL - AFSP SGS TUV Saar Gmbh

Website https://sgs-tuev-saar.com/en/trainings-certifications/certifications/certificate-database/persons/type/afse

AUTOMOTIVE CYBERSECURITY PROFESSIONAL - CACSP SGS TUV Saar Gmbh

Website https://sgs-tuev-saar.com/en/trainings-certifications/certifications/certificate-database/persons/type/cacsp

Delhi, India

PROJECT MANAGEMENT IIT DELHI

Website https://home.iitd.ac.in/

CURRENT

ASEP - SYSTEMS ENGINEERING PROFESSIONAL INCOSE

SAFE AGILIST Scaled Agile inc.

LANGUAGE SKILLS

Other language(s):

	UNDERSTANDING		SPEAKING		WRITING
	Listening	Reading	Spoken production	Spoken interaction	
ENGLISH	C1	C1	C1	C1	C1

Levels: A1 and A2: Basic user; B1 and B2: Independent user; C1 and C2: Proficient user

SKILLS

Microsoft Office package: Microsoft Word, Excel, PowerPoint, Access | program firmware | define software architecture | lead a team | use software design patterns | design firmware | Agile project management | firmware | embedded systems | develop ICT device driver | analyse software specifications | ICT communications protocols | debug software | Eclipse (integrated development environment software)

HONOURS AND AWARDS

01/04/2009

Erasmus Mundus Master of Science in Photonics – Belgium

Belgium Government fellowship for Masters of Science in Photonics engineering in 2009