PRASADRAM SHRISHA

shpra18@gmail.com +91 9158499418 https://www.linkedin.com/in/pr-shrisha/

SUMMARY

- About 19+ years of experience in safety critical embedded SW development for global product R&D.
- Looking for senior roles in Technical and Engineering leadership.

EXPERIENCE

SW Architect, L&T Technology Services (Sep 2024 to Dec 2024)

- Managed 12-member team in defining SYS level requirements in DOORS DNG for the Vehicle/Safety functions, static and dynamic architecture definition in Rhapsody / mapping/ updating Interface signals (ETH / SOME- IP). Interfaced with cross functional global teams for PI planning on the ART, collaborated for IBM EWM ALM workflow integration along with leading the local sprints. The Zonal E/E architecture has combined AUTOSAR Adaptive and Classic ECUs connected via Ethernet. The platform ECU is based on multi-core CPU running QNX Hypervisor. Acquired IBM Rhapsody specialist certification for SysML V8.

Sr. TECHNICAL ARCHITECT, HCLTech (Jan 2019 to Sep 2024)

- Specified the SW architecture, provided hands on technical leadership to a team of 3-4 members in implementing UDS protocol (ISO 14229) on a legacy ECU based on Renesas RH850. Refined the existing CAN driver, reused CAN-Tp layer from legacy platform, delivered 30% ahead of time and reduced development costs by 60%.

- Created preliminary outline SW designs for Software components (SW-C) Test SWC, COM Error Handler SWC for handling the CAN timeout errors. This quick PoC led to increased customer confidence on creating new SW-Cs at Application layer.

Sr. TECHNICAL ARCHITECT, HCLTech JAPAN (Aug 2019 to Apr 2021)

- Stationed at OEM location in Japan as SW - Architect / onsite coordinator on development/Acceptance test topics in a V-cycle. Awarded Individual Best Performer by customer for architecture/ code deliveries for year 2020.

- Enhanced the legacy platform SW architecture by façade design pattern-based HAL for Platform SW, ported freeRTOS on RH850 based ECU, improved platform SW by adding abstraction layer over the real time kernel.

- Designed threadsafe and re-entrant middleware SW libraries on Freescale iMX257 target ECU / µITRON4 kernel for Tractor HMIs.Created SW Safety analyses as per IEC 61784-3 Functional safety fieldbuses for CAN communications black channel in Stairlift elevator product firmware (SIL 2).

SW ARCHITECT, ALSTOM TRANSPORT (Jun 2017 to Dec 2018)

- Built and managed a team of 4 members for the SIL4 SW Integration tests for Test campaign on Alpha releases.

- Created Application protocols architecture concept and safety layer black channel (EN 50159). Platform is Safety computer having 2 x (2 Out Of 2) Composite fail safe dual channel architecture running on Multicore CPU / PikeOS Hypervisor with Time / Space partitioning. Product: Alstom CBTC solution U400 with CENELEC EN 50128 / RAMS

- Provided technical leadership to a team of 3 developers in developing a M out of N(MooN) Simulator as LXC container- based PC App that emulated the actual SIL4 Safety computer.

MANAGER I Firmware, SIEMENS (Sep 2011 to Jun 2017)

FIRMWARE ARCHITECT (Apr 2015 to Jun 2017)

- Defined a preliminary SW architecture for integration of LoRa radio module /LoRaWAN protocol stack to the Fault passage indicator (FPI) - used to detect phase faults and earth faults in medium-voltage cable networks.

- Technically led a team in prototyping using Semtech SX1278 COTS. Ported Micrium µCOSIII III kernel on a Freescale Kinetis K10 target for new bring up. As Re-use correspondent for global Embedded SW Re-use project, closely collaborated with PO/Architects in Germany for SW Architecture, COTS/legacy SW re use libraries deployment in Design to Cost (DTC) projects.

PRINCIPAL ENGINEER- SW, SIEMENS UNITED KINGDOM (Mar 2013 to Apr 2015)

- Created hardware abstraction layer for Tricore / Cortex M4 custom HW, introduced RTOS support in platform software by defining OSAL, ported and integrated freeRTOS, analysed and fixed PR / CRs on Platform and Communication SW components in legacy Control & Protection devices (Reyrolle/Siprotec branded Intelligent Electronic Devices).

- Long-term deputation to UK R&D Centre aimed at technical transfer of SIEMENS Control & Protection products with UK and German teams.

FIRMWARE MANAGER, SIEMENS (Oct 2011 to Mar 2013)

- Technically lead a team of 8 developers for developing fail safe voter redundancy, embedded webserver apps and integrating Comm.stack (SMSC lan92xx ETH chip /Fusion TCP/IP stack/HTTP stack, IEC 60870-5-104,101 libraries) middleware/application, customised rules in PC Lint for Blackfin DSP builds.

- The SW/HW development relies on the SICAM CMIC module (RTUs used for Secondary Distribution Automation) based Redundancy solution used for Turbine control applications that are redundant, with high-availability and fault-tolerant / safety integrity levels up to SIL2 (IEC 61508). As SubPM -Firmware, successfully performed insourcing of Feeder RTU from 3rd party contractors, sustenance and enhancement activities and NPI/NPD.

- Worked on a long term in Siemens Austria on SW architecture definition and development tasks in accordance to SIL2 (IEC 61508), ported Micrium µCOSII Real time kernel on Blackfin DSP, developed platform SW and COM stacks. Built from scratch the firmware team and ramped up team size to 20, identified 3rd party COTS libraries for make/buy decisions that led to improved platform sustenance. The projects used an Agile-LEAN techniques for NPI/NPD/Sustenance.

Sr. Engineer (R&D), CE+T POWER (Mar 2010 to Sep 2011)

- Implemented CANopen protocol using stack from PORT Gmbh, optimised CPU cycles by 3x and achieved small code size by 2x, developed CANopen bootloader via Service data objects (SDO) upload/download mechanism. Developed modBUS and CAN management modules and integrated into the Inverter codebase.

- Worked in Belgium on a long term for SW development/Integration work packages. End product is a Modular inverter with N+1 redundancy for telecom applications.

SR. SW ENGINEER, ABB CORPORATE RESEARCH (Jul 2005 to Oct 2008)

- Designed Vxworks drivers for SPI flash and RS485, optimized driver functionality by adding handling echo, collision avoidance / detection and resend for interrupt driven scenario with 2-wire mode.

- Developed Distributed Network Protocol (DNP3) stack using C++/Vxworks 5.5 on a PowerPC target, implemented observer design pattern for the protocol event subsystem, designed middleware libraries for Trend/Alarm handling subsystem, unit tested achieving 90% coverage.

- Worked for a long term in Sweden for development/SW integration. Products: Power System protection Substation Automation Products ABB REx670, TEC, 800xA ABB Distributed Control Systems

ENGINEER - Design & Development, TATA Elxsi (Dec 2004 to Jun 2005)

- Developed threadsafe re-entrant libraries for RTP/RTSP multithreaded applications on ARM9 / Linux / WIN32.

SW ENGINEER, L&T EmSyS (Jul 2004 to Oct 2004)

- Enhanced platform SW on Vxworks 5.4/ PowerPC custom target / Diab C for Firmware sustenance tasks on medical devices.

RESEARCH ENGINEER FELLOW, DRDO (Feb 2003 to Jul 2004)

- Developed and technically documented platform SW low level drivers in Vxworks 5.4 / PowerPC for Aerospace systems in a controlled DoD-STD-2167A process for LCA (Light Combat Aircraft) program.

EDUCATION

- PG Certificate Embedded Systems Design, University of Pune, India, B+ Grade
- Bachelor of Engineering (Electronics & Instrumentation), R V College of Engineering (TIER I), First Class

CONTINUOUS LEARNING & PROFESSIONAL CERTIFICATIONS

- Automotive Cybersecurity Professional (CACSP) certification valid till (up to 04.07.2029) – Znumber 1294
https://sgs-tuev-saar.com/en/trainings-certifications/certifications/certificate-database/persons/type/cacsp
- Automotive Functional Safety (AFSP) professional certification (up to 25.05.2029) – Znumber 4714
https://sgs-tuev-saar.com/en/trainings-certifications/certifications/certificate-database/persons/type/afse
- Certified People Manager, HCLTech, 2023
- Safety SW Product Architectures, ALSTOM, 2018
- Certified SAFe Agilist, Scaled Agile Inc., since Aug 2018
- CEP Certificate course in Project Management, IIT Delhi / PMCC - 2018

AWARDS & SCHOLARSHIP

Government of India Scholar- Belgium Government Fellowship for higher studies in Electronics Engineering - 2009

SKILLS

C, C++, Assembly,RTOS, Vxworks, freeRTOS, RH850,NXPS32k,Microcontrollers, Hypervisor, Lauterbach, TRACE32, SysML, Rhapsody, Atlassian Confluence, IBM DOORS Next(DNG), ISO 26262, ISO 21434, Micrium, , Power PC, ARM Cortex, Blackfin DSP, Firmware, Embedded Software, Multicore, AutoSAR, GENy, MCAL BSW, CAN-FD,UDS,CAN, ECU, Automotive Ethernet, SOME/IP, CAN, Can-FD, J1939, CANopen, USB, Bootloaders, Multithreading, Debugging, Multi-core, Device Drivers, Protocol stack, MISRA C, Polyspace QA-C, ClearCase, ClearQuest, GIT, Jazz RTC,IBM EWM ALM, Industrial Automation, Energy Management, CENELEC,EN50128, File Systems, Reuse, Delivery Manager, Project Management, SAFe Agilist , PMP, Software Architecture, Middleware, HAL, Vector, Da Vinci, ARXML, AutoSAR Configuration, SW Architecture, Technical leadership, People management, Onsite Coordination, PC-Lint, Functional Safety, Cybersecurity, ClearCase, ClearQuest, Protection Relays, Feeder RTU, DNP3, IEC60870-5-104, fieldbus, Modbus, Distribution Automation IEC 61508, DCS, Platform SW, Communication Protocols, IoT